Instruction Manual

Tektronix

TMS 231
MC3X0 Microprocessor Support

071-0891-00

www.tektronix.com

Tektronix, Inc., P.O. Box 500, Beaverton, OR 97077

SOFTWARE WARRANTY

Tektronix warrants that the media on which this software product is furnished and the encoding of the programs on the media will be free from defects in materials and workmanship for a period of three (3) months from the date of shipment. If a medium or encoding proves defective during the warranty period, Tektronix will provide a replacement in exchange for the defective medium. Except as to the media on which this software product is furnished, this software product is provided “as is” without warranty of any kind, either express or implied. Tektronix does not warrant that the functions contained in this software product will meet Customer’s requirements or that the operation of the programs will be uninterrupted or error-free.

In order to obtain service under this warranty, Customer must notify Tektronix of the defect before the expiration of the warranty period. If Tektronix is unable to provide a replacement that is free from defects in materials and workmanship within a reasonable time thereafter, Customer may terminate the license for this software product and return this software product and any associated materials for credit or refund.

THIS WARRANTY IS GIVEN BY TEKTRONIX IN LIEU OF ANY OTHER WARRANTIES, EXPRESS OR IMPLIED. TEKTRONIX AND ITS VENDORS DISCLAIM ANY IMPLIED WARRANTIES OF MERCHANTABILITY OR FITNESS FOR A PARTICULAR PURPOSE. TEKTRONIX’ RESPONSIBILITY TO REPLACE DEFECTIVE MEDIA OR REFUND CUSTOMER’S PAYMENT IS THE SOLE AND EXCLUSIVE REMEDY PROVIDED TO THE CUSTOMER FOR BREACH OF THIS WARRANTY. TEKTRONIX AND ITS VENDORS WILL NOT BE LIABLE FOR ANY INDIRECT, SPECIAL, INCIDENTAL, OR CONSEQUENTIAL DAMAGES IRRESPECTIVE OF WHETHER TEKTRONIX OR THE VENDOR HAS ADVANCE NOTICE OF THE POSSIBILITY OF SUCH DAMAGES.

Table of Contents

Reference

Index

List of Figures

List of Tables

General Safety Summary

Review the following safety precautions to avoid injury and prevent damage to this product or any products connected to it. To avoid potential hazards, use this product only as specified.

While using this product, you may need to access other parts of the system. Read the *General Safety Summary* in other system manuals for warnings and cautions related to operating the system.

Symbols and Terms

Terms in this Manual. These terms may appear in this manual:

WARNING. *Warning statements identify conditions or practices that could result in injury or loss of life.*

CAUTION. *Caution statements identify conditions or practices that could result in damage to this product or other property.*

Terms on the Product. These terms may appear on the product:

DANGER indicates an injury hazard immediately accessible as you read the marking.

WARNING indicates an injury hazard not immediately accessible as you read the marking.

CAUTION indicates a hazard to property including the product.

Symbols on the Product. The following symbols may appear on the product:

CAUTION
Refer to Manual

Preface

This instruction manual contains specific information about the TMS231 MC3X0 microprocessor support package and is part of a set of information on how to operate this product on compatible Tektronix logic analyzers.

If you are familiar with operating microprocessor support packages on the logic analyzer for which the TMS231 MC3X0 support was purchased, you will only need this instruction manual to set up and run the support.

If you are not familiar with operating microprocessor support packages, you will need to supplement this instruction manual with information on basic operations to set up and run the support. See Manual Conventions below for more information.

Manual Conventions

This manual uses the following conventions:

- The term “disassembler” refers to the software that disassembles bus cycles into instruction mnemonics and cycle types.
- The phrase “information on basic operations” refers to your online help or a user manual covering the basic operations of microprocessor support.

Contacting Tektronix

Phone	1-800-833-9200*
Address	Tektronix, Inc. Department or name (if known) 14200 SW Karl Braun Drive P.O. Box 500 Beaverton, OR 97077 USA
Web site	www.tektronix.com
Sales support	1-800-833-9200, select option 1*
Service support	1-800-833-9200, select option 2*
Technical support	Email: techsupport@tektronix.com 1-800-833-9200, select option 3* 1-503-627-2400 6:00 a.m. – 5:00 p.m. Pacific time

*** This phone number is toll free in North America. After office hours, please leave a voice mail message.**
Outside North America, contact a Tektronix sales office or distributor; see the Tektronix web site for a list of offices.

Getting Started

Getting Started

This section contains information on the TMS231 MC3X0 microprocessor support package and on connecting your logic analyzer to your system under test.

Support Package Description

The TMS231 MC3X0 microprocessor support package displays disassembled data from systems based on the MCORE MC3X0 microprocessor.

To use this support efficiently, you need to have the items listed in the information on basic operations and *M3X0 User Manual*, M340 Specification v1.1, 11/20/98.

Information on basic operations also contains a general description of support.

Logic Analyzer Software Compatibility

The floppy disk label on the microprocessor support states which version of logic analyzer software this support is compatible with.

Logic Analyzer Configuration

The TMS231 MC3X0 support requires a minimum of one 102-channel module.

Requirements and Restrictions

You should review the general requirements and restrictions of microprocessor support packages as they pertain to your system under test.

You should also review electrical specifications in *Specifications* on page 3–1 as they pertain to your system under test, as well as the following descriptions of other MC3X0 support requirements and restrictions.

System Clock Rate

The operating speeds that the MC3X0 support can acquire data from the MC3X0 microprocessor are listed on Table 3–1. These specifications were valid at the time this manual was printed. Please contact your Tektronix Sales Representative for current information on the fastest devices supported.

NonIntrusive Acquisition

Acquiring microprocessor bus cycles is nonintrusive to the system under test. That is, the MC3X0 support does not intercept, modify, or present signals back to the system under test.

Disabling the Instruction Cache

To display disassembled acquired data, you must disable the internal instruction cache. Disabling the cache makes all instruction prefetches visible on the bus so they can be acquired and displayed disassembled.

Limitation of the Support

8 Bit Mode

In 8 bit mode if the Data comes in higher than 3 bytes D[31:24], D[23:16] and D[15:8] it is not supported.

Multiple Instructions

If multiple Branch instructions and MultiRead/Write instructions are entering the fetch queue then the TMS231 MC3X0 support may not disassemble correctly. In these cases the Mark Opcode Option can be used for correct disassembly.

Functionality Not Tested

- RIM mode
- 16 bit Upper and Lower modes
- 8 bit mode

Since the modes for RIM, 16 bit Upper and Lower, and 8 bit are not tested, even though they are supported, the disassembly may be incorrect.

Connecting the Logic Analyzer to a System Under Test

You can use channel probes, clock probes, and leadsets with a commercial test clip (or adapter) to make connections between the logic analyzer and your system under test.

To connect the probes to MC3X0 signals in the system under test using a test clip, follow these steps:

1. Power off your system under test. It is not necessary to power off the logic analyzer.

CAUTION. *To prevent static damage, handle the microprocessor, the probes, and the logic analyzer module components only in a static-free environment. Static discharge can damage these components.*

Always wear a grounding wrist strap, heel strap, or similar device while handling the microprocessor.

2. To discharge your stored static electricity, touch the ground connector located on the back of the logic analyzer. If you are using a test clip, touch any of the ground pins on the clip to discharge stored static electricity from the test clip.

CAUTION. *To prevent damage to the pins on the microprocessor, place the system under test on a horizontal surface before connecting the test clip.*

3. Place the system under test on a horizontal static-free surface.
4. Use Tables 5–2 through 5–12 beginning on page 5–3 to connect the channel probes to MC3X0 signal pins on the test clip or in the system under test.

   Use leadsets to connect at least one ground lead from each channel probe and the ground lead from each clock probe to ground pins on your test clip.

Operating Basics

Setting Up the Support

The information in this section is specific to the operations and functions of the TMS231 MC3X0 microprocessor support on any Tektronix logic analyzer for which it can be purchased.

Before you acquire and display disassembled data, you need to load the support and specify setups for clocking and triggering as described in the information on basic operations in your logic analyzer online help. The microprocessor support provides default values for each of these setups as well as user-definable settings.

Installing the Support Software

NOTE. *Before you install any software, it is recommended that you verify that the microprocessor support software is compatible with the logic analyzer software.*

To install the TMS231 MC3X0 software on your Tektronix logic analyzer, follow these steps:

1. Insert the floppy disk in the disk drive.
2. Click the Windows Start button, point to Settings, and click Control Panel.
3. In the Control Panel window, double-click Add/Remove Programs.
4. Follow the instructions on the screen for installing the software from the floppy disk.

To remove or uninstall software, close all windows, and then follow the above instructions and select Uninstall.

Channel Group Definitions

The software automatically defines channel groups for the support. The channel groups for the TMS231 MC3X0 support are Address, Data, Control, Chip Select, Proc_Mode, Interrupt, and Misc. The channel group tables begin on page 5–1.

Support Package Setups

The TMS231 MC3X0 software installs MC3X0 support package setup file.

MC3X0 Setup This setup provides disassembly support. Signals are displayed as they appear electrically on the front side bus.

Clocking

Options The TMS231 MC3X0 support offers a microprocessor-specific clocking mode for the MC3X0 microprocessor. This clocking mode is the default selection whenever you load the TMS231 MC3X0 support.

Disassembly is not correct when using the Internal or External clocking modes. Information on basic operations in your online help describes in more detail how to use these clock selections for general purpose analysis.

- Internal clocking is used for timing and is based on the clock generated by a Tektronix logic analyzer. You can configure the clock rate from 50 ms down to 4 ns resolution.
- External clocking is used when you configure the clocking of data based on logical combinations of clocks and qualifiers.

Custom Clocking

When Custom is selected, the Custom Clocking Options menu has the subtitle MC3X0 Microprocessor Clocking Support added, and the clocking options are also displayed.

The TMS231 MC3X0 support has three clocking options.

- MC3X0 _RIM
- MC3X0 _EIM
- MC3X0 _CORE(MLB)

After loading the MC3X0 support and choosing one of the previous clocking options, the following disassembly support selections are available. These Disassembly support selections are defined based on the actual control signals available to the system under test.

Disassembly support selections:

- Use Control Signals Default (most accurate disassembly)
- Clock Edge With R/W~
- Clock Edge Without R/W~

MC3X0 _RIM

Use Control Signals (Default). The Use Control Signals selection acquires signals (RST~, OE~, TA~ and SHS~) with the greatest amount of accuracy. Signals are sampled at every clock edge when the control signals are active. The master strobe occurs when the clock signal line changes from low to high. Figure 2–1 shows the sample point and master sample point for acquiring the signals.

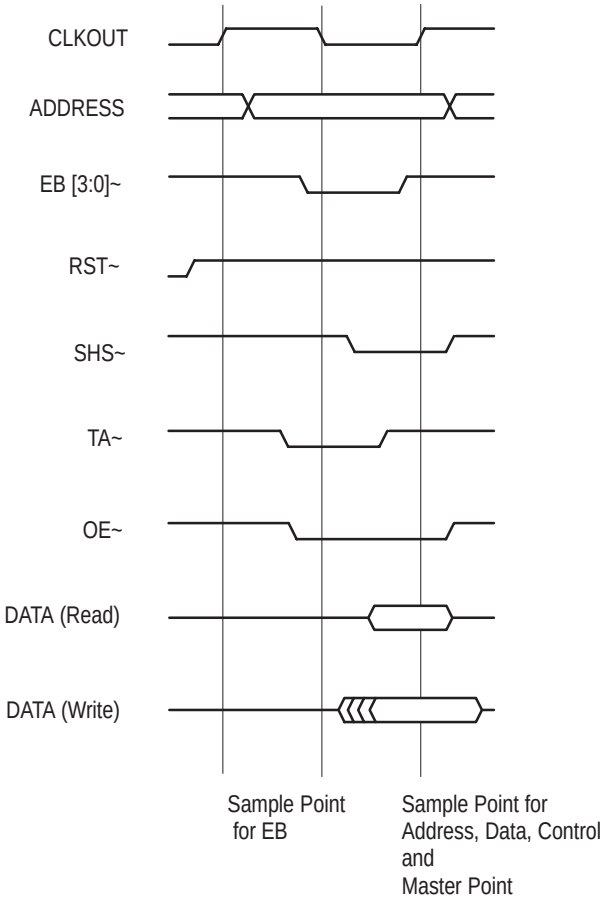

Figure 2–1: MC3X0 _RIM sample point and master sample point

Clock Edge With R/W~. The Clock Edge With R/W~ is best used when you want to distinguish a read cycle from a write cycle, even though extra data is saved that may cause errors in the disassembly. With this selection, signals are acquired at every clock cycle without any qualifier. On every falling edge Byte Enable signals are sampled and on every rising edge Address, Control, and Data signals are sampled and saved.

Clock Edge Without R/W~. The Clock Edge Without R/W~ is best used when you have not aquired control signals for acquisition.

Signals are acquired at every clock cycle without any qualifier. On every falling edge Byte Enable signals are sampled and on every rising edge Address, Control and Data signals are sampled and saved. This selection does not distinguish a read cycle from a write cycle so extra data is saved that may cause errors in the disassembly.

MC3X0 _EIM

Use Control Signals (Default). The Use Control Signals selection acquires signals with the greatest amount of accuracy. Signals are sampled at every rising clock edge when the control signals (RST~, OE~ and R/W~) are active. The master strobe occurs when the clock signal line changes from low to high. Figure 2–2 shows the sample point and master sample point for acquiring the signals.

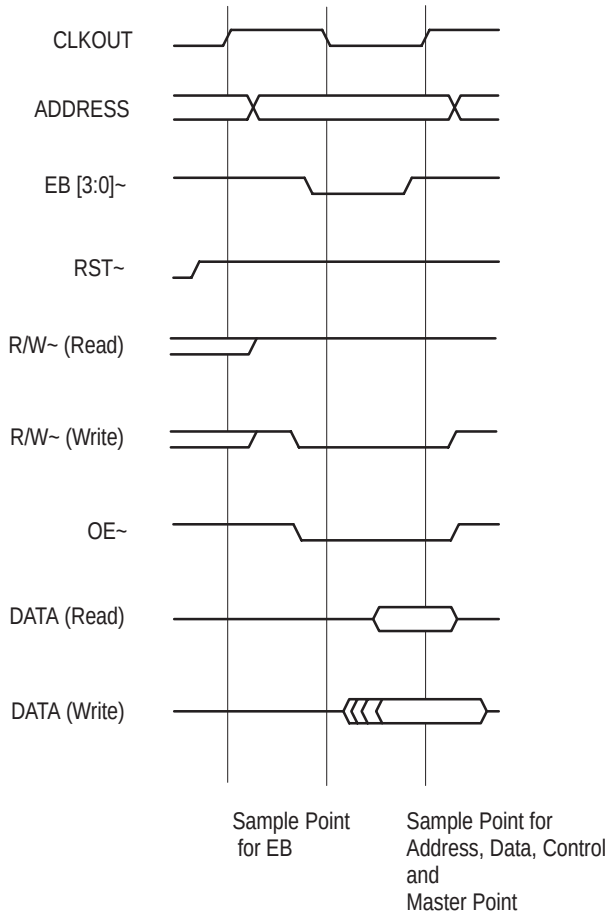

Figure 2–2: MC3X0 _EIM sample point and master sample point

Clock Edge With R/W~. The Clock Edge With R/W~ is best used when you want to distinguish a read cycle from a write cycle; unfortunately, this selection saves extra data causing errors in the disassembly. With this selection, signals are acquired at every clock cycle without any qualifier. On every falling edge Byte Enable signals are sampled and on every rising edge Address, Control, and Data signals are sampled and saved.

Clock Edge Without R/W~. The Clock Edge Without R/W~ is best used when you have not acquired control signals for acquisition.

Signals are acquired at every clock cycle without any qualifier. On every falling edge Byte Enable signals are sampled and on every rising edge the Address, Control and Data signals are sampled and saved. This selection does not distinguish a read cycle from a write cycle, extra data is saved that may cause errors in the disassembly.

MC3X0_CORE(MLB)

Use Control Signals (Default). The Use Control Signals selection acquires signals with the greatest amount of accuracy. Signals are sampled at every rising clock edge when the control signals (RST~, TREQ~ and TA~) are active. The master strobe occurs when the clock signal line changes from low to high. Figure 2–3 shows the sample point and master sample point for acquiring the signals.

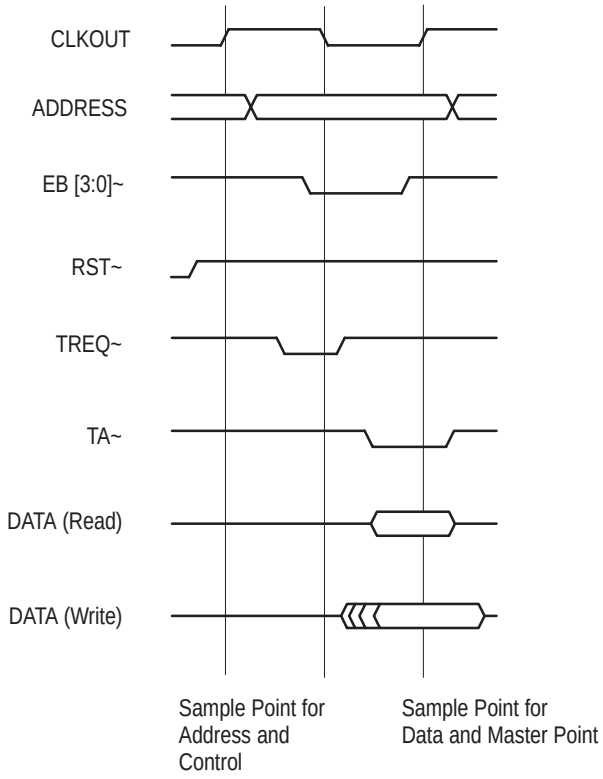

Figure 2–3: MC3X0 _CORE(MLB) sample point and master sample point

Clock Edge With R/W~. The Clock Edge With R/W~selection is best used when you want to distinguish a read cycle from a write cycle; unfortunately, this selection saves extra data causing errors in the disassembly. With this selection, signals are acquired at every clock cycle without any qualifier. On every falling edge, Address and Control signals are sampled and on every rising edge Data signals are sampled and saved.

Clock Edge Without R/W~. The Clock Edge Without R/W~ is best used when you have not acquired control signals for acquisition.

Signals are acquired at every clock cycle without any qualifier. On every falling edge Address and Control signals are sampled and on every rising edge Data signals are sampled and saved. This selection does not distinguish a read cycle from a write cycle, so extra data is saved that may cause errors in the disassembly.

Setup and Hold Time. You can change the Setup and Hold time window of all the signal groups. The default Setup time is 2.5 ns and the Hold time is 0 ns. The Setup and Hold that you defined has precedence over any default Setup and Hold time.

Acquiring and Viewing Disassembled Data

Acquiring Data

Once you load the TMS231 MC3X0 support, choose a clocking mode, and specify the trigger, you are ready to acquire and disassemble data.

If you have any problems acquiring data, refer to information on basic operations in your logic analyzer online help or *Appendix A: Error Messages and Disassembly Problems* in your logic analyzer user manual.

Viewing Disassembled Data

You can view disassembled data in six display formats: Timing, State, Hardware, Software, Control Flow, and Subroutine. The information on basic operations describes how to select the disassembly display formats.

NOTE. *Selections in the Disassembly property page (the Disassembly Format Definition overlay) must be set correctly for your acquired data to be disassembled correctly. Refer to* Changing How Data is Displayed *on page 2–12.*

The default display format displays the Address, Data, Control, Proc_Mode, ChipSelect, and Interrupt channel group values for each sample of acquired data along with Sample, Mnemonic, and Timestamp.

Any channel group or display column can be made visible by selecting the Add column option in the Disassembly property page.

The disassembler displays special characters and strings in the instruction mnemonics to indicate significant events. Table 2–1 lists these special characters and strings and gives a definition of what they represent.

Table 2–1: Description of special characters in the display

Character or string displayed	Definition
#	Indicates an immediate value.
>	Indicates that there is sufficient room on the screen to show all available data.
>> On the TLA 700	Indicates that the instruction was manually marked as a program fetch.

Table 2–1: Description of special characters in the display (cont.)

Character or string displayed	Definition
t	Indicates the number shown is in decimal, such as #12t.
****	Indicates that there is insufficient data available for complete disassembly of the instruction; the number of asterisks indicates the width of the data that is unavailable. Each two asterisks represent one byte.

Timing Display Format

The Timing-Waveform display format file is provided for the TLA 700 Series support. The timing-waveform display format file sets up and displays the following waveforms:

CLKOUT
Address (busform)
Data (busform)
RST~
R/W~
OE~
EB~[0:3]
CS~[1:4]

Hardware Display Format

In Hardware display format, the disassembler displays certain cycle type labels in parentheses. Table 2–2 lists cycle type labels and gives a definition of the cycle they represent. Reads to interrupt and exception vectors are labeled with the vector name.

Table 2–2: Cycle type labels and definitions

Cycle Type	Definition
(RESET)	Indicates system RESET
(DATA RETRIEVAL ERROR)	Indicates invalid DATA READ cycle
(READ)	Indicates DATE READ cycle
(WRITE)	Indicates DATE WRITE cycle
(EXTENSION)	Indicates an extension to a preceding instruction opcode
(FLUSH)	Indicates a cycle was fetched but not executed
(READ or WRITE)	Indicates a noninstruction sequence when R/W~ is not used
(UNKNOWN)	Indicates a combination of control bits are unexpected or unrecognized

Figure 2–4 shows an example of a Hardware display.

Sample	MC3X0 Address	MC3X0 Data	MC3X0 Mnemonics		MC3X0 Control
	00401016	----6022	MOVI	R2,#02	READ
5	00401018	6044----	MOVI	R4,#04	READ
	0040101A	----2070	ADDI	R0,#08	READ
6	0040101C	1254----	MOV	R4,R5	READ
	0040101E	----F7F0	BR	00401000	READ
7	00401020	0042C000	(FLUSH)		READ
8	00401000	01E4----	ABS	R4	READ
	00401002	----C1E0	ABS	R0	READ
9	00401004	01E7----	ABS	R7	READ
	00401006	----F001	BR	0040100A	READ
10	00401008	12107105	(FLUSH)		READ
11	0040100A	----7105	LRW	R1,[00401020]	READ
12	0040100C	3601----	BTSTI	R1,#00	READ
	0040100E	----F802	BSR	00401014	READ
13	00401020	0042C000	(READ)		READ
14	00401010	60226023	(FLUSH)		READ
15	00401014	2470----	SUBI	R0,#08	READ
	00401016	----6022	MOVI	R2,#02	READ
16	00401018	6044----	MOVI	R4,#04	READ
	0040101A	----2070	ADDI	R0,#08	READ
17	0040101C	1254----	MOV	R4,R5	READ
	0040101E	----F7F0	BR	00401000	READ
18	00401020	0042C000	(FLUSH)		READ
19	00401000	01E4----	ABS	R4	READ
	00401002	----C1E0	ABS	R0	READ
20	00401004	01E7----	ABS	R7	READ

Figure 2–4: Hardware display format

Software Display Format

The Software display format displays only the first fetch of executed instructions. Flushed cycles and extensions are not shown, even though they are part of the executed instruction. Read extensions are used to disassemble the instruction, but they are not displayed as a separate cycle in the Software display format. Data reads and writes are not displayed.

Control Flow Display Format

The Control Flow display format displays only the first fetch of instructions that cause a branch in the addressing and special cycles to change the flow of control.

Instructions that generate a change in the flow of control in the MC3X0 microprocessor are as follows:

BF	Branch on condition false
BR	Branch
BT	Branch on condition true
JMP	Jump
JMPI	Jump indirect

Subroutine Display Format

The Subroutine display format displays only the first fetch of subroutine call or return instructions. It can display conditional subroutine calls if they are considered to be taken.

Instructions that generate a subroutine call or a return in the MC3X0 microprocessor are as follows:

BSR	Branch on subroutine
JSR	Jump to subroutine
JMP	Jump
JSRI	Jump to subroutine indirect
RTE	Return from exception
RFI	Return from interrupt
BKPT	Break Point
TRAP	Trap

Changing How Data is Displayed

Common fields and features allow you to further modify displayed data to suit your needs. You can make common and optional display selections in the Disassembly property page (the Disassembly Format Definition overlay).

Optional Display Selections

You can make optional selections for acquired disassembled data. In addition to the common selections (described in the information on basic operations), you can change the displayed data in the following ways:

Show:	Hardware	(default)
	Software	
	Control Flow	
	Subroutine	
Highlight:	Software	(default)
	Control Flow	
	Subroutine	
	None	
Disasm Across Gaps:		No (default)
		Yes

Micro-Specific Fields

Endian Mode. Indicate the MC3X0 processor configuration for viewing data from memory in the following order:

Little Endian	(default)
Big Endian	

Interface. Select the interface type:

RIM	(default)
EIM	
CORE(MLB)	

Data Port Width. Indicate the data port width:

32-bit port	(default)
16-bit port (D15:D0)	
16-bit port (D31:D16)	
8-bit port (D7:D0)	

R/W~ Signal. Indicate whether the R/W~ signal is available:

Available	(default)
Not Available	

CS Mode. Indicate whether the Chip select CS[0:5] signals are available in the system:

CS Available	(default)
Not Available	

Vector Base Register. Enter the base address of the Interrupt Vector table:

0x00000000	(default)

RIM CS1 Base Address. Enter the base address for the Chip select (CS1) for RIM Interface:

0x00000000	(default)

RIM CS2 Base Address. Enter the base address for the Chip select (CS1) for RIM Interface:

0x00000000	(default)

RIM CS3 Base Address. Enter the base address for the Chip select (CS1) for RIM Interface:

0x00000000 (default)

RIM CS4 Base Address. Enter the base address for the Chip select (CS1) for RIM Interface:

0x00000000 (default)

Marking Cycles

The TMS231 MC3X0 support allows marks on potential instruction fetch cycles (which includes read extensions and flush cycles.) Cycle marks are not available if the cursor is placed on other cycle marks. To place a cycle mark use the Mark Opcode button. The Mark Opcode button functions when disassembly is available.

If the cycle being marked, is not a potential instruction fetch cycle (which includes read extensions and flush cycles), the Mark Opcode selections are replaced by a note indicating that "An Opcode Mark cannot be placed at the selected data sample."

When a cycle is marked, this character, >>, is displayed immediately to the left of the Mnemonics column. Cycles can be unmarked by using the Undo Mark selection, which removes this character, >>. If more than one set of sequences are marked, then the you can undo the marks using the Remove all Marks option.

The following cycle marks are available for instruction fetch cycles in the 8 bit Data Port:

Opcode	Marks the cycle as an instruction opcode
Extension	Marks the cycle as an extension to an instruction opcode
Flush	Marks the cycle as a flushed cycle
Read	Marks the cycle as a read cycle (if the R/W~ signal is not available)
Write	Marks the cycle as a write cycle (if the R/W~ signal is not available)
Undo Mark	Removes all marks from the current sample

The following cycle marks are available for instruction fetch cycles in the 16 bit Data Port:

Opcode	Marks the cycle as an instruction opcode
Read	Marks the cycle as a read cycle (if the R/W~ signal is not available)
Write	Marks the cycle as a write cycle (if the R/W~ signal is not available)

Flush	Marks the cycle as a flushed cycle
Undo Mark	Removes all marks from the current sample

The following cycle marks are available for instruction fetch cycles in the 32 bit Data Port:

Opcode_Opcode	Marks the cycle as an instruction opcode and opcode
Opcode_Flush	Marks the cycle as an instruction opcode and flush
Flush_Opcode	Marks the cycle as a flush and instruction opcode
Extension	Marks the cycle as an extension to an instruction opcode
Flush	Marks the cycle as a flushed cycle
Read	Marks the cycle as a read cycle (if the R/W~ signal is not available)
Write	Marks the cycle as a write cycle (if the R/W~ signal is not available)
Undo Mark	Removes all marks from the current sample

Displaying Exception Labels

The disassembler can display TMS231 MC3X0 exception labels. The exception table must reside in external memory for interrupt and exception cycles to be visible to the disassembler.

You can enter the table prefix in the Exception Prefix field. The Exception Prefix field provides the disassembler with the offset address; enter a three-digit hexadecimal value corresponding to the prefix of the exception table.

These fields are located in the Disassembly property page (Dissembled Format Definition overlay).

Table 2–3 lists the TMS231 MC3X0 interrupt and exception labels.

Table 2–3: Interrupt and exception labels

Vector Number	Offset	Displayed interrupt or exception name
0	0x000	(RESET)
1	0x004	(MISALIGNED ACCESS)
2	0x008	(ACCESS ERROR)
3	0x00C	(DIVIDE BY ZERO)
4	0x010	(ILLEGAL INSTRUCTION)
5	0x014	(PRIVILEGE VIOLATION)
6	0x018	(TRACE EXCEPTION)
7	0x01C	(BREAKPOINT EXCEPTION)

Table 2–3: Interrupt and exception labels (Cont.)

Vector Number	Offset	Displayed interrupt or exception name
8	0x020	(UNRECOVERABLE ERROR)
9	0x024	(Idly4 ERROR)
10	0x028	(INT AUTOVECTOR)
11	0x02C	(FINT AUTOVECTOR)
12	0x030	(RESERVED (HAI))
13	0x034	(RESERVED (FP))
14	0x038	(TLB INST MISS EXCEPTION)
15	0x03C	(TLB DATA MISS EXCEPTION)
16 to 19	0x040 to 0x04C	(TRAP #0 TO 3 INSTRUCTION VECTOR)
20 to 30	0x050 to 0x078	(RESERVED)
31	0x07C	(SYSTEM DESCRIPTOR POINTER)
32 to 127	0x080 to 0x1FC	(RESERVED)

Viewing an Example of Disassembled Data

A demonstration system file (or demonstration reference memory) is provided on your MC3X0 software support disk so you can see an example of how your MC3X0 microprocessor bus cycles and instruction mnemonics look when they are disassembled. Viewing the system file is not a requirement for preparing the module for use. You can view the system file without connecting the logic analyzer to your system under test.

Specifications

Specifications

This section contains information regarding the specifications of the TMS231 MC3X0 microprocessor support.

Specification Tables

Tables 3–1 list the electrical requirements that the system under test must produce for the TMS231 MC3X0 support to acquire correct data.

Table 3–1: Electrical specifications

Characteristics	Requirements
System under test clock rate	
Maximum specified clock rate:	100 MHz
Tested clock rate *	100 MHz
Minimum setup time required	2.5 ns
Minimum hold time required	0 ns

*** Please contact your Tektronix Sales Representative for current information on the tested clock rate.**

Replaceable Parts

Replaceable Parts

This section contains a list of the replaceable components for the TMS231 MC3X0 hardware support product.

Parts Ordering Information

Replacement parts are available through your local Tektronix field office or representative.

Changes to Tektronix products are sometimes made to accommodate improved components as they become available and to give you the benefit of the latest improvements. Therefore, when ordering parts, it is important to include the following information in your order:

- Part number
- Instrument type or model number
- Instrument serial number
- Instrument modification number, if applicable

If you order a part that has been replaced with a different or improved part, your local Tektronix field office or representative will contact you concerning any change in part number.

Change information, if any, is located at the rear of this manual.

Using the Replaceable Parts List

The tabular information in the Replaceable Parts List is arranged for quick retrieval. Understanding the structure and features of the list will help you find all of the information you need for ordering replacement parts. The following table describes the content of each column in the parts list.

Parts list column descriptions

Column	Column name	Description
1	Figure & index number	Items in this section are referenced by figure and index numbers to the exploded view illustrations that follow.
2	Tektronix part number	Use this part number when ordering replacement parts from Tektronix.
3 and 4	Serial number	Column three indicates the serial number at which the part was first effective. Column four indicates the serial number at which the part was discontinued. No entries indicates the part is good for all serial numbers.
5	Qty	This indicates the quantity of parts used.
6	Name & description	An item name is separated from the description by a colon (:). Because of space limitations, an item name may sometimes appear as incomplete. Use the U.S. Federal Catalog handbook H6-1 for further item name identification.
7	Mfr. code	This indicates the code of the actual manufacturer of the part.
8	Mfr. part number	This indicates the actual manufacturer's or vendor's part number.

Abbreviations

Abbreviations conform to American National Standard ANSI Y1.1–1972.

Chassis Parts

Chassis-mounted parts and cable assemblies are located at the end of the Replaceable Electrical Parts List.

Mfr. Code to Manufacturer Cross Index

The table titled Manufacturers Cross Index shows codes, names, and addresses of manufacturers or vendors of components listed in the parts list.

Manufacturers cross index

Mfr. code	Manufacturer	Address	City, state, zip code
TK2548	XEROX CORPORATION	14181 SW MILLIKAN WAY	BEAVERTON, OR 97005

Replaceable parts list

Fig. & index number	Tektronix part number	Serial no. effective	Serial no. discont'd	Qty	Name & description	Mfr. code	Mfr. part number
					STANDARD ACCESSORIES		
	071-0891-00			1	MANUAL, TECH: INSTRUCTIONS, MC3X0, TMS231	TK2548	071-0891-00

Reference

Reference: Tables

This section lists the Symbol table and the Channel group tables for disassembly and timing.

Symbol Table

Table 5–1 lists the name, bit pattern, and meaning for the symbols in the file MC3X0_Ctrl, the Control channel group symbol table.

Table 5–1: MC3X0 _Ctrl group symbol table definitions

Symbol	Control group value										Meaning
	RST~	TEA~	R/W~	TSIZ1	TSIZ0	OE~	EB3~	EB2~	EB1~	EB0~	
RESET	0	X	X	X	X	X	X	X	X	X	RESET
DATA_RETR_ERR	1	0	X	X	X	X	X	X	X	X	Data Retrieval Error
WRITE	1	1	0	X	X	X	X	X	X	X	Data Write
READ	1	1	1	X	X	X	X	X	X	X	Data Read
UNKNOWN	X	X	X	X	X	X	X	X	X	X	Unknown

Channel Assignments

Channel assignments listed in Tables 5–2 through 5–8 use the following conventions:

- All signals are required by the support unless indicated otherwise.
- Channels are listed starting with the most significant bit (MSB), descending to the least significant bit (LSB).
- Channel group assignments are for all modules unless otherwise noted.
- A tilde symbol (~) following a signal name indicates an active low signal.
- An equals symbol (=) following a signal name indicates that it is double probed.
- The module in the lower-numbered slot is referred to as the HI module and the module in the lower-numbered slot is referred to as the LO module.

  The portable logic analyzer has the lower-numbered slots on the top, and the benchtop logic analyzer has the lower-numbered slots on the left.

The channel assignment groups are displayed in the following order:

Group name	Display radix
Address	Hexadecimal
Data	Hexadecimal
Mnemonic	None
Control	Symbolic
Chip_select	BIN
Proc_Mode	BIN
Interrupt	BIN
Misc	Off

Table 5–2 lists the probe section and channel assignments for the Address group and the microprocessor signal to which each channel connects. By default the Address channel group assignments are displayed in hexadecimal.

Table 5–2: Address channel group assignments

Bit order	Section:channel	MC3X0 signal name
31	A3:7	A31
30	A3:6	A30
29	A3:5	A29
28	A3:4	A28
27	A3:3	A27
26	A3:2	A26
25	A3:1	A25
24	A3:0	A24
23	A2:7	A23
22	A2:6	A22
21	A2:5	A21
20	A2:4	A20
19	A2:3	A19
18	A2:2	A18
17	A2:1	A17
16	A2:0	A16
15	A1:7	A15
14	A1:6	A14
13	A1:5	A13
12	A1:4	A12
11	A1:3	A11
10	A1:2	A10
9	A1:1	A9
8	A1:0	A8
7	A0:7	A7
6	A0:6	A6
5	A0:5	A5
4	A0:4	A4
3	A0:3	A3
2	A0:2	A2
1	A0:1	A1
0	A0:0	A0

Table 5–3 lists the probe section and channel assignments for the Data group and the microprocessor signal to which each channel connects. By default the Data channel group assignments are displayed in hexadecimal.

Table 5–3: Data channel group assignments

Bit order	Section:channel	MC3X0 signal name
31	D3:7	D31
30	D3:6	D30
29	D3:5	D29
28	D3:4	D28
27	D3:3	D27
26	D3:2	D26
25	D3:1	D25
24	D3:0	D24
23	D2:7	D23
22	D2:6	D22
21	D2:5	D21
20	D2:4	D20
19	D2:3	D19
18	D2:2	D18
17	D2:1	D17
16	D2:0	D16
15	D1:7	D15
14	D1:6	D14
13	D1:5	D13
12	D1:4	D12
11	D1:3	D11
10	D1:2	D10
9	D1:1	D9
8	D1:0	D8
7	D0:7	D7
6	D0:6	D6
5	D0:5	D5
4	D0:4	D4
3	D0:3	D3
2	D0:2	D2
1	D0:1	D1
0	D0:0	D0

Table 5–4 lists the probe section and channel assignments for the Proc_Mode group and the microprocessor signal to which each channel connects. The default radix of the Proc_Mode group is Binary on the logic analyzer.

Table 5–4: Proc_Mode channel group assignments

Bit order	Section:channel	MC3X0 signal name
10	C2:7	PSTAT3
9	C2:6	PSTAT2
8	C2:5	PSTAT1
7	C2:4	PSTAT0
6	C3:6	TC2
5	C3:5	TC1
4	C3:4	TC0
3	C1:7	SEQ~
2	C1:2	BIGEND~
1	C1:0	IFETCH
0	C1:6	BURST~\BAA~

Table 5–5 lists the probe section and channel assignments for the Control group and the microprocessor signal to which each channel connects. The default radix of the Control group is Symbolic on the logic analyzer. The symbol table file name is MC3X0_Ctrl.

Table 5–5: Control channel group assignments

Bit order	Section:channel	MC3X0 signal name
9	C2:3	RST~
8	C3:7	TEA~
7	C2:2	R/W~
6	C3:3	TSIZ1
5	C3:2	TSIZ0
4	C2:1	OE~*
3	C0:7	EB3~*
2	C0:6	EB2~*
1	C0:5	EB1~*
0	C0:4	EB0~*

*** Indicates the signal is supported by RIM and EIM interface**

By default, Chip_Select channel group assignments in Table 5–6 are shown displayed as binary.

Table 5–6: Chip_Select channel group assignments

Bit order	Section:channel	MC3X0 signal name
5	C1:5	CS5~ †
4	C1:4	CS4~*
3	C0:3	CS3~*
2	C0:2	CS2~*
1	C0:1	CS1~*
0	C0:0	CS0~ †

***** **Indicates the signal is supported by RIM and EIM interface**

† **Indicates the signal is supported by EIM interface**

By default, Interrupt channel group assignments in Table 5–7 are displayed as binary.

Table 5–7: Interrupt channel group assignments

Bit order	Section:channel	MC3X0 signal name
1	C3:1	FINT~
0	C3:0	INT~

By default, Misc channel group assignments listed in Table 5–8 are not displayed.

Table 5–8: Misc channel group assignments

Bit order	Section:channel	MC3X0 signal name
5	Clock:3	TREQ~
4	C2:0	TBUSY~
3	C1:3	ABORT~
2	Clock:2	SHS~
1	Clock:1	TA~
0	C1:1	RSTOUT~

Table 5–9 lists the probe section and clock and qualifier channel assignments. The clock probes are not part of any group.

Table 5–9: Clock and Qualifier channel assignments

Section:channel	MC3X0 signal name	Comments
CLK:0	CLKOUT	–
CLK:1	TA~	–
CLK:2	SHS~	–
CLK:3	TREQ~	–
C2:0	TBUSY~	–
C2:1	OE~	–
C2:2	R/W~	–
C2:3	RST~	–
QUAL:0	Not used	102 & 136 channel
QUAL:1	Not used	102 & 136 channel
QUAL:2	Not used	136 channel only
QUAL:3	Not used	136 channel only

Acquisition Setup. The TMS231 MC3X0 support affects the logic analyzer setup menus (and submenus) by modifying existing fields and adding micro-specific fields.

The TMS231 MC3X0 support adds the selection MC3X0 to the Load Support Package dialog box, under the File pulldown menu. After the MC3X0 support is loaded, the Custom clocking mode selection in the module Setup menu is enabled.

Table 5–10 lists the signals required for Clock and Disassembly.

Table 5–10: Signals required for clocking and disassembly

Section:channel	MC3X0 signal name
A31–A24	A3
A23–A16	A2
A15–A8	A1
A7–A0	A0
D31–D24	D3
D23–D16	D2
D15–D8	D1
D7–D0	D0
CLKOUT	Clock:0
TA~	Clock:1
SHS~	Clock:2
TREQ~	Clock:3
CS5~	C1:5
CS4~	C1:4
CS3~	C0:3
CS2~	C0:2
CS1~	C0:1
CS0~	C0:0
RST~	C2:3
TEA~	C3:7
R/W~	C2:2
TSIZ1	C3:3
TSIZ0	C3:2
OE~	C2:1
EB3~	C0:7
EB2~	C0:6
EB1~	C0:5
EB0~	C0:4
PSTAT3	C2:7
PSTAT2	C2:6
PSTAT1	C2:5

Table 5–10: Signals required for clocking and disassembly (cont.)

Section:channel	MC3X0 signal name
PSTAT0	C2:4
TC2	C3:6
TC1	C3:5
TC0	C3:4
SEQ~	C1:7
BIGEND~	C1:2
IFETCH	C1:0
BURST~\BAA~	C1:6
FINT~	C3:1
INT~	C3:0

Table 5–11 lists the signals not required for Clock and Disassembly.

Table 5–11: Signals not required for clocking and disassembly

Section:channel	MC3X0 signal name
TBUSY~	C2:0
ABORT~	C1:3
RSTOUT~	C1:1

CPU To Mictor Connections

To probe the microprocessor you need to make connections between the CPU and the Mictor pins of the P6434 Mass Termination Probe. Refer to the *P6434 Mass Termination Probe* manual, Tektronix part number 070-9793-xx, for more information on mechanical specifications. Tables 5–12 through 5–14 list the CPU pin to Mictor pin connections.

Tektronix uses a counterclockwise pin assignment. Pin 1 is located at the top left, and pin 2 is located directly below it. Pin 20 is located on the bottom right, and pin 21 is located directly above it.

AMP uses an odd side-even side pin assignment. Pin 1 is located at the top left, and pin 3 is located directly below it. Pin 2 is located on the top right, and pin 4 is located directly below it (see Figure 5–1).

NOTE. *When designing Mictor connectors into your system under test, always follow the Tektronix pin assignment.*

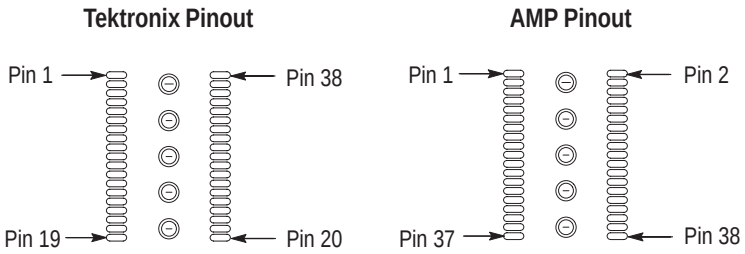

Figure 5–1: Pin assignments for a Mictor connector (component side)

CAUTION. *To protect the CPU and the inputs of the module, it is recommended that a 180 Ω resistor be connected in series between each ball pad of the CPU and each pin of the Mictor connector. The resistor must be within 1/2 inch of the ball pad of the CPU.*

Table 5–12: CPU to Mictor connections for clock and qualifiers

LA channel	MC3X0 signal name	Tektronix mictor C pin number	AMP mictor C pin number
Clock:3	TREQ~	C3	C5
Clock:2 QUAL	SHS~	D36	D6
Clock:1 QUAL	TA~	A36	A6
Clock:0 CLK	CLKOUT	A3	A5
QUAL:3	—	—	—
QUAL:2	—	—	—
QUAL:1	—	—	—
QUAL:0	—	—	—

Table 5–13: CPU to Mictor connections for Mictor A pins

Logic analyzer channel	MC3X0 signal name	Tektronix mictor A pin number	AMP mictor A pin number
A0:0	A0	A20	A38
A0:1	A1	A21	A36
A0:2	A2	A22	A34
A0:3	A3	A23	A32
A0:4	A4	A24	A30
A0:5	A5	A25	A28
A0:6	A6	A26	A26
A0:7	A7	A27	A24
A1:0	A8	A28	A22
A1:1	A9	A29	A20
A1:2	A10	A30	A18
A1:3	A11	A31	A16
A1:4	A12	A32	A14
A1:5	A13	A33	A12
A1:6	A14	A34	A10
A1:7	A15	A35	A8
A2:0	A16	A19	A37

Table 5–13: CPU to Mictor connections for Mictor A pins (cont.)

Logic analyzer channel	MC3X0 signal name	Tektronix mictor A pin number	AMP mictor A pin number
A2:1	A17	A18	A35
A2:2	A18	A17	A33
A2:3	A19	A16	A31
A2:4	A20	A15	A29
A2:5	A21	A14	A27
A2:6	A22	A13	A25
A2:7	A23	A12	A23
A3:0	A24	A11	A21
A3:1	A25	A10	A19
A3:2	A26	A9	A17
A3:3	A27	A8	A15
A3:4	A28	A7	A13
A3:5	A29	A6	A11
A3:6	A30	A5	A9
A3:7	A31	A4	A7

Table 5–14: CPU to Mictor connections for Mictor D pins

LA channel	MC3X0 signal name	Tektronix mictor D pin number	AMP mictor D pin number
D0:0	D0	D20	D38
D0:1	D1	D21	D36
D0:2	D2	D22	D34
D0:3	D3	D23	D32
D0:4	D4	D24	D30
D0:5	D5	D25	D28
D0:6	D6	D26	D26
D0:7	D7	D27	D24
D1:0	D8	D28	D22
D1:1	D9	D29	D20

Table 5–14: CPU to Mictor connections for Mictor D pins (cont.)

LA channel	MC3X0 signal name	Tektronix mictor D pin number	AMP mictor D pin number
D1:2	D10	D30	D18
D1:3	D11	D31	D16
D1:4	D12	D32	D14
D1:5	D13	D33	D12
D1:6	D14	D34	D10
D1:7	D15	D35	D8
D2:0	D16	D19	D37
D2:1	D17	D18	D35
D2:2	D18	D17	D33
D2:3	D19	D16	D31
D2:4	D20	D15	D29
D2:5	D21	D14	D27
D2:6	D22	D13	D25
D2:7	D23	D12	D23
D3:0	D24	D11	D21
D3:1	D25	D10	D19
D3:2	D26	D9	D17
D3:3	D27	D8	D15
D3:4	D28	D7	D13
D3:5	D29	D6	D11
D3:6	D30	D5	D9
D3:7	D31	D4	D7

Table 5–15: CPU to Mictor connections for Mictor C pins

LA channel	MC3X0 signal name	Tektronix mictor C pin number	AMP mictor C pin number
C3:7	TEA~	C4	C7
C3:6	TC2	C5	C9
C3:5	TC1	C6	C11

Table 5–15: CPU to Mictor connections for Mictor C pins (cont.)

LA channel	MC3X0 signal name	Tektronix mictor C pin number	AMP mictor C pin number
C3:4	TC0	C7	C13
C3:3	TSIZ1	C8	C15
C3:2	TSIZ0	C9	C17
C3:1	FINT~	C10	C19
C3:0	INT~	C11	C21
C2:7	PSTAT3	C12	C23
C2:6	PSTAT2	C13	C25
C2:5	PSTAT1	C14	C27
C2:4	PSTAT0	C15	C29
C2:3 (Qual)	RST~	C16	C31
C2:2 (Qual)	R/W~	C17	C33
C2:1 (Qual)	OE~	C18	C35
C2:0 (Qual)	TBUSY~	C19	C37
C1:7	SEQ~	C35	C8
C1:6	BURST~\BAA~	C34	C10
C1:5	CS5~	C33	C12
C1:4	CS4~	C32	C14
C1:3	ABORT~	C31	C16
C1:2	BIGEND~	C30	C18
C1:1	RSTOUT~	C29	C20
C1:0	IFETCH	C28	C22
C0:7	EB3~	C27	C24
C0:6	EB2~	C26	C26
C0:5	EB1~	C25	C28
C0:4	EB0~	C24	C30
C0:3	CS3~	C23	C32
C0:2	CS2~	C22	C34
C0:1	CS1~	C21	C36
C0:0	CS0~	C20	C38

Index

Index

I

L

M

P

R

S

T

U

V

W